

Fig. 1

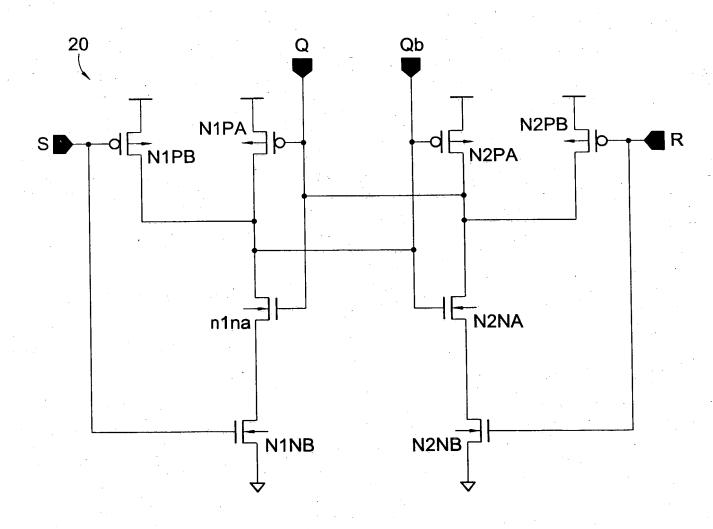
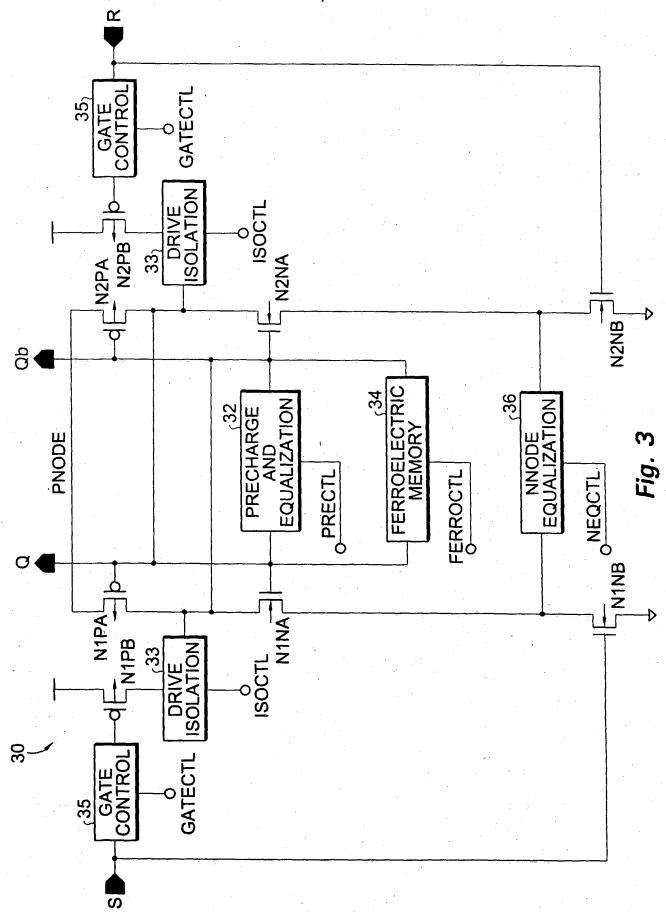
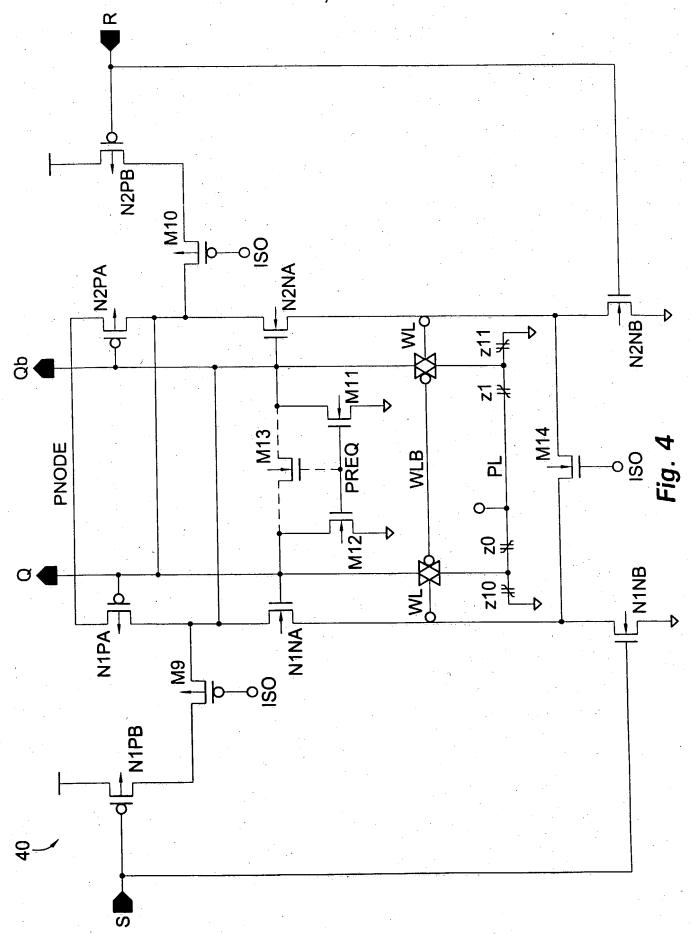
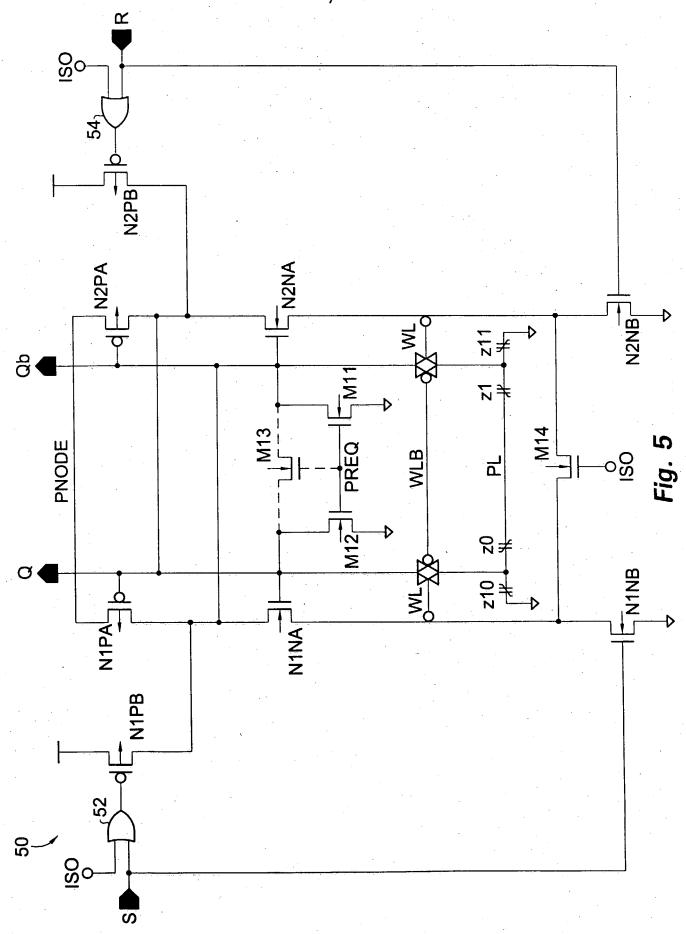


Fig. 2







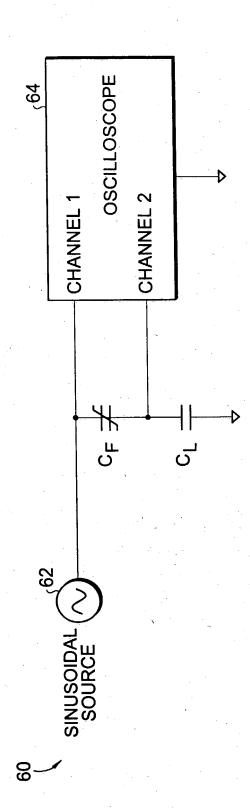


FIG. 0

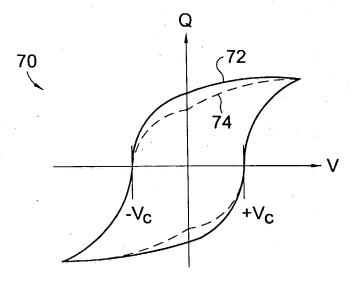


Fig. 7

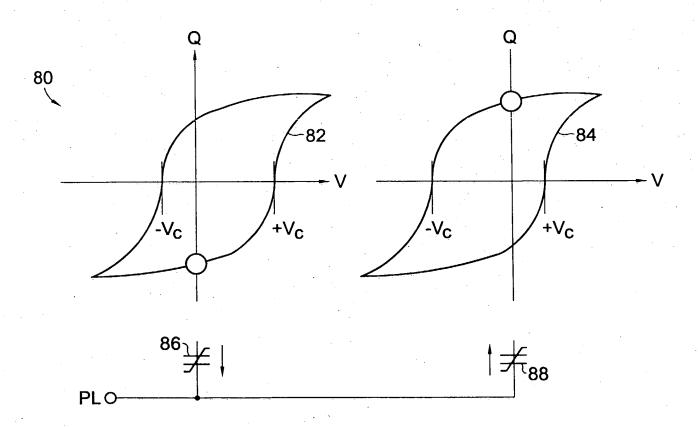


Fig. 8

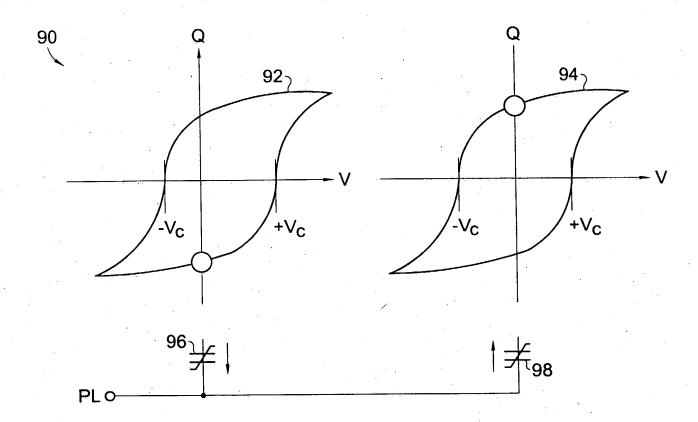
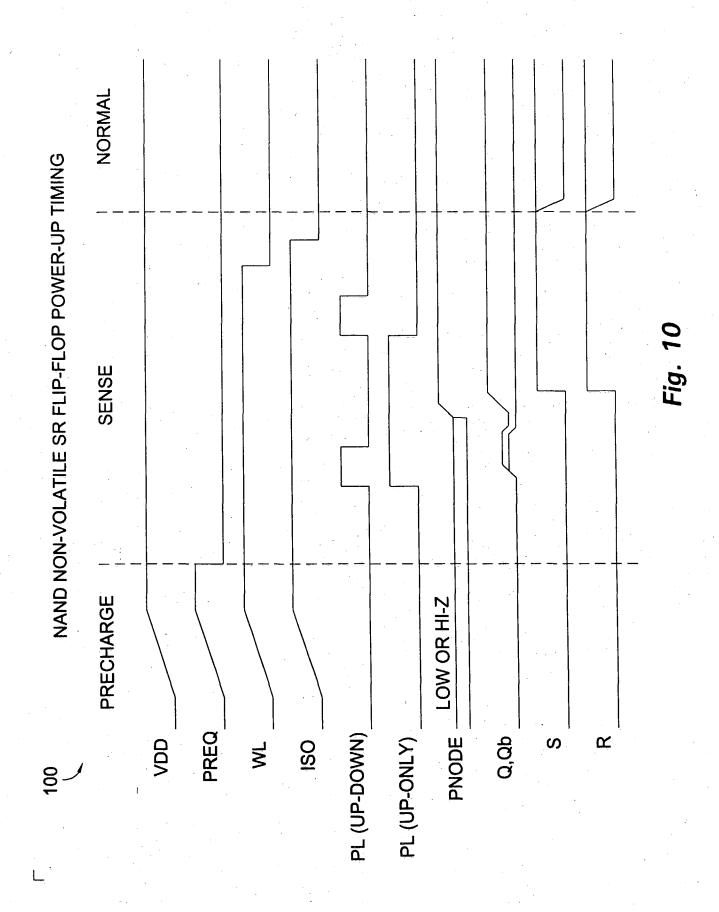
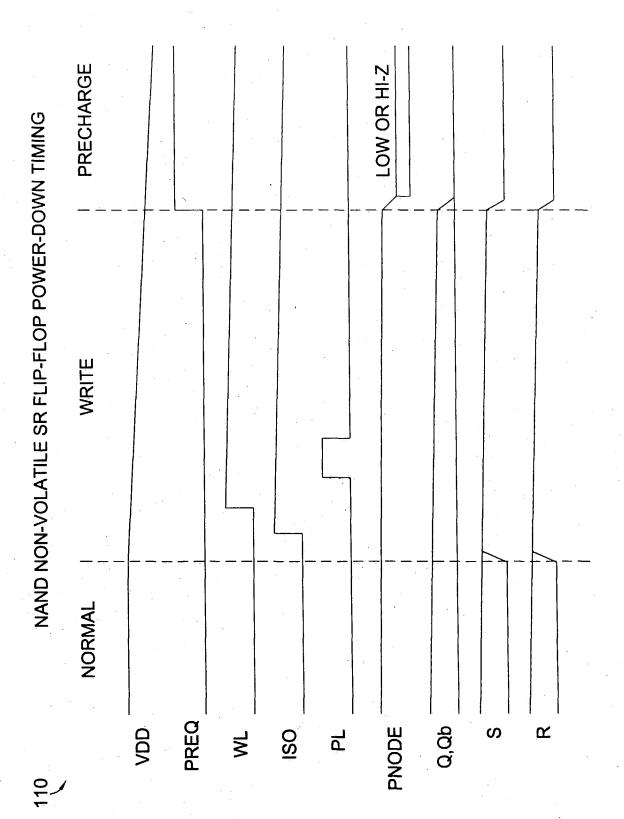


Fig. 9





Fia. 11

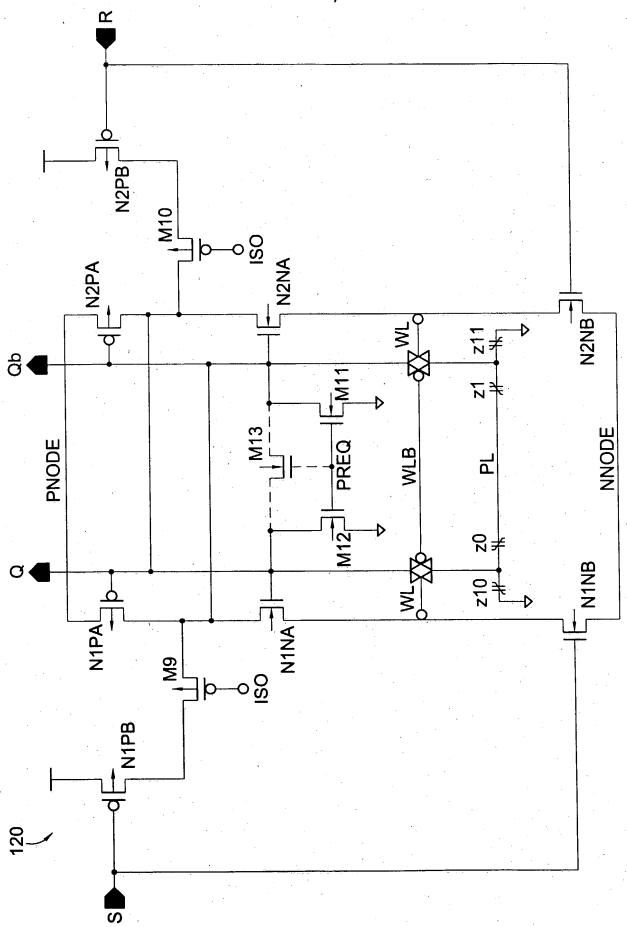


Fig. 12A

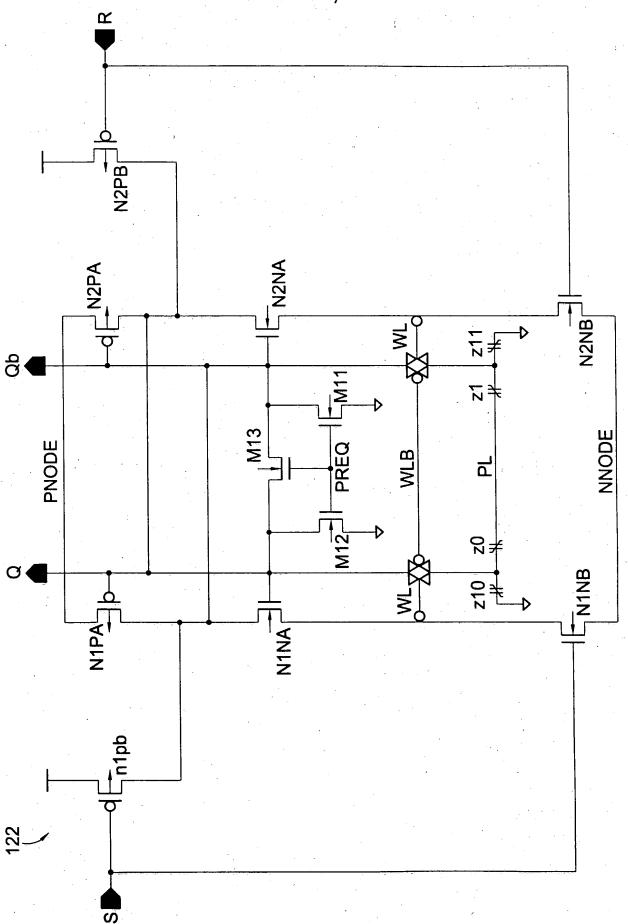
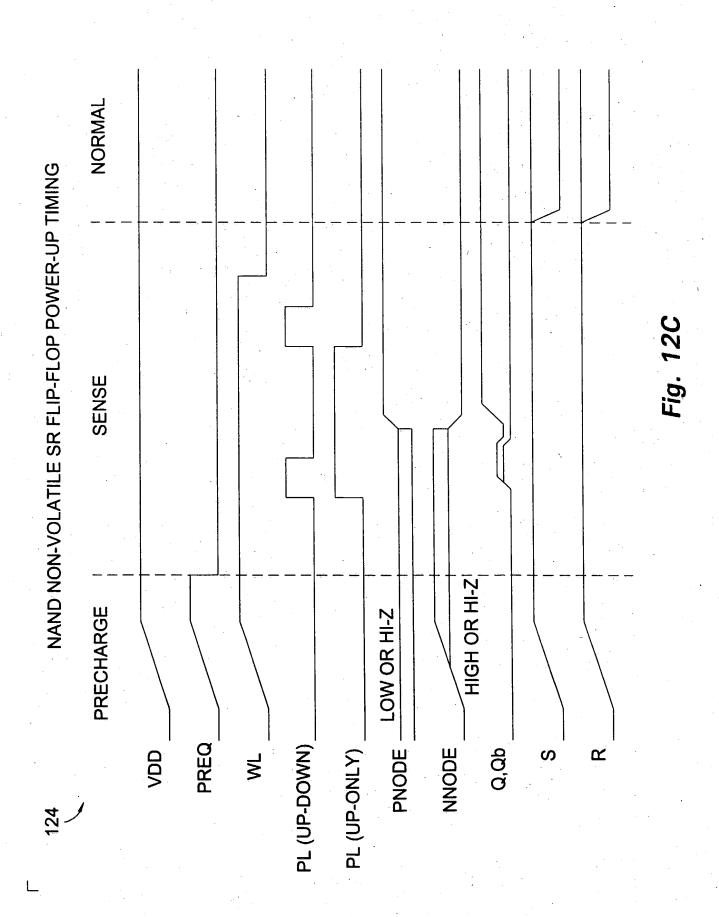


Fig. 12B



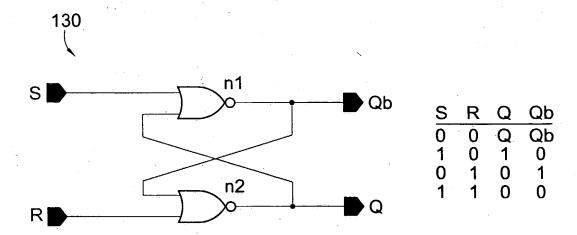


Fig. 13

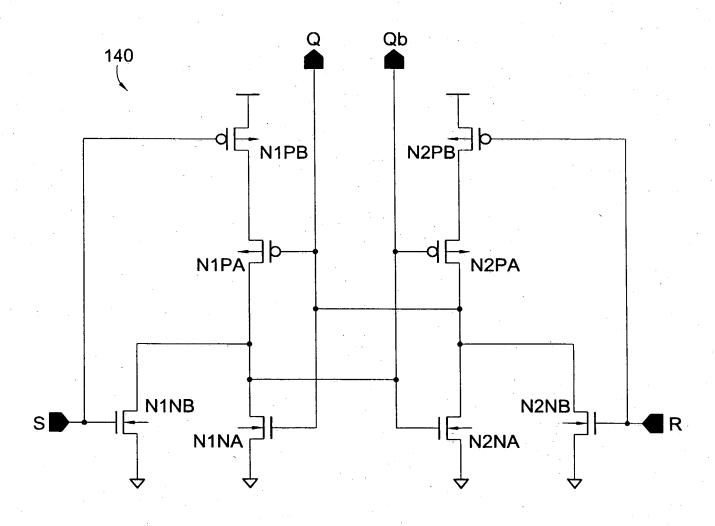
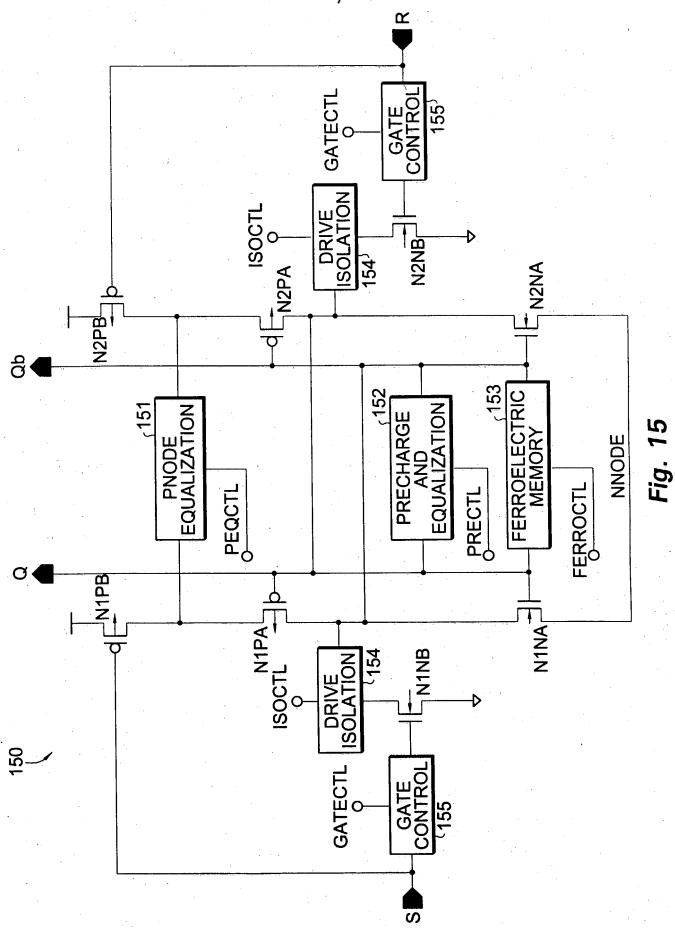
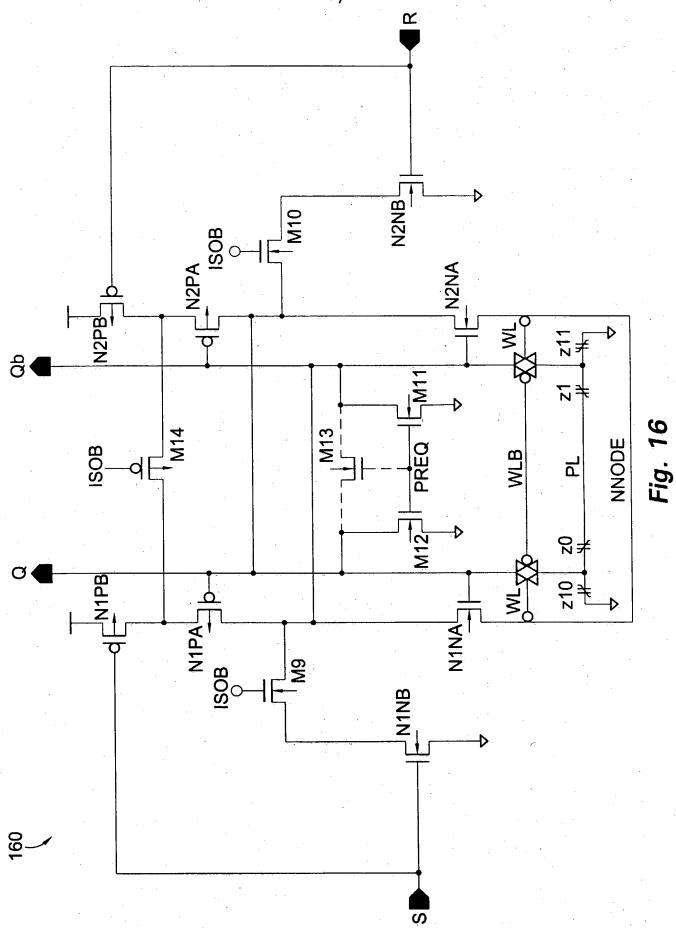
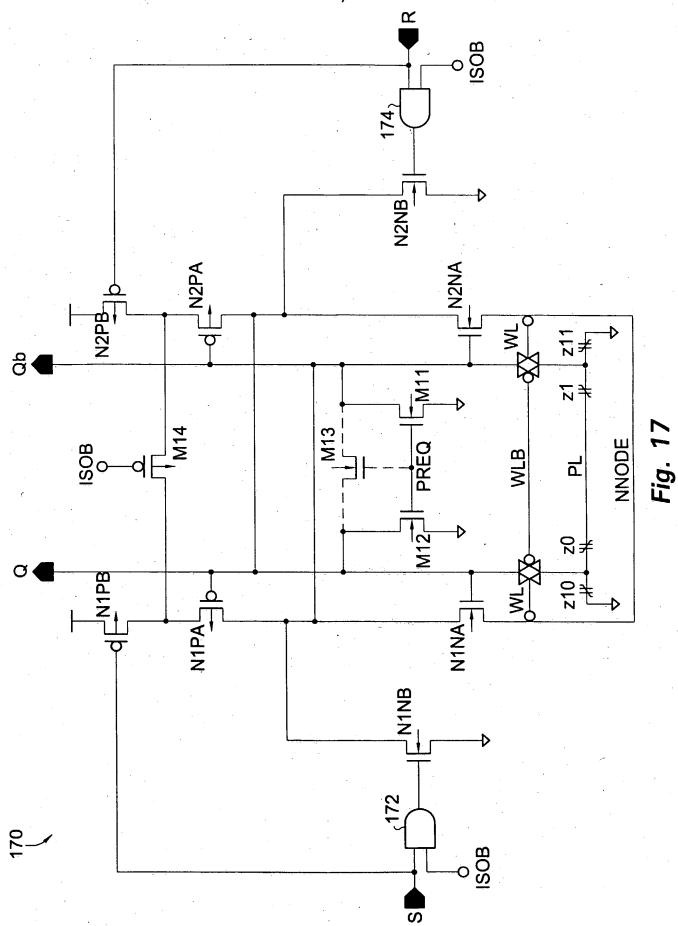
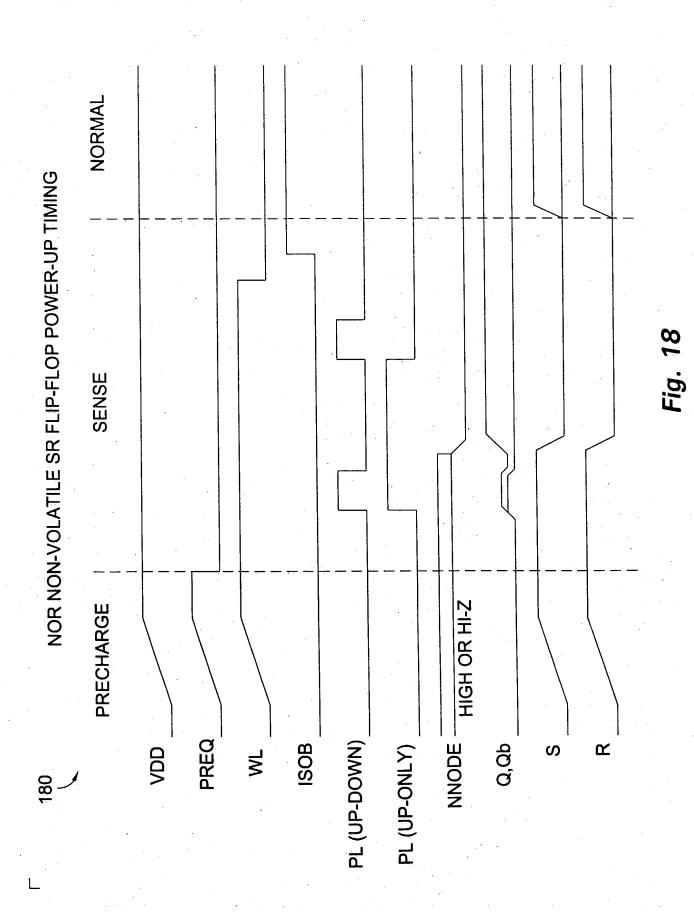


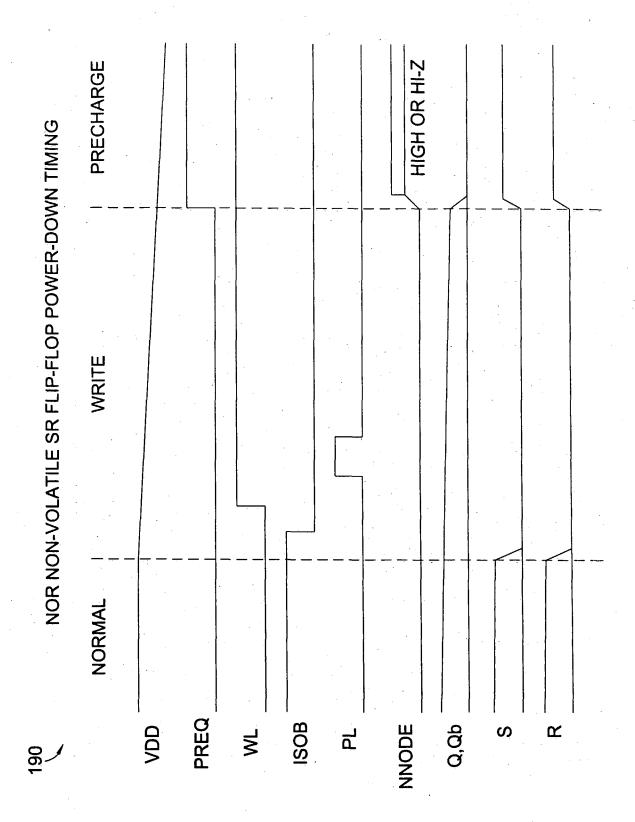
Fig. 14











Fia. 19

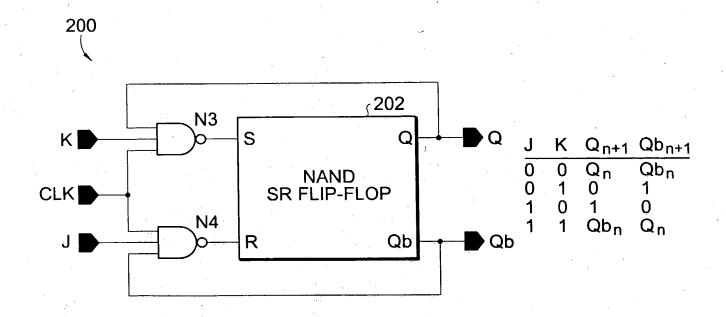


Fig. 20

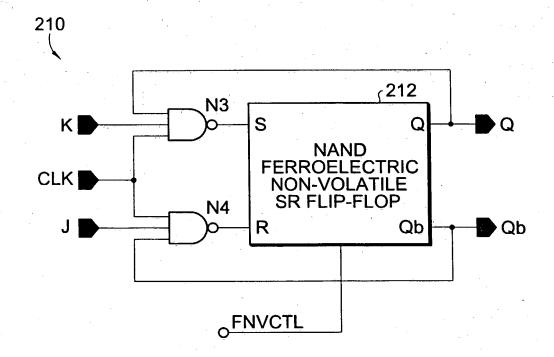
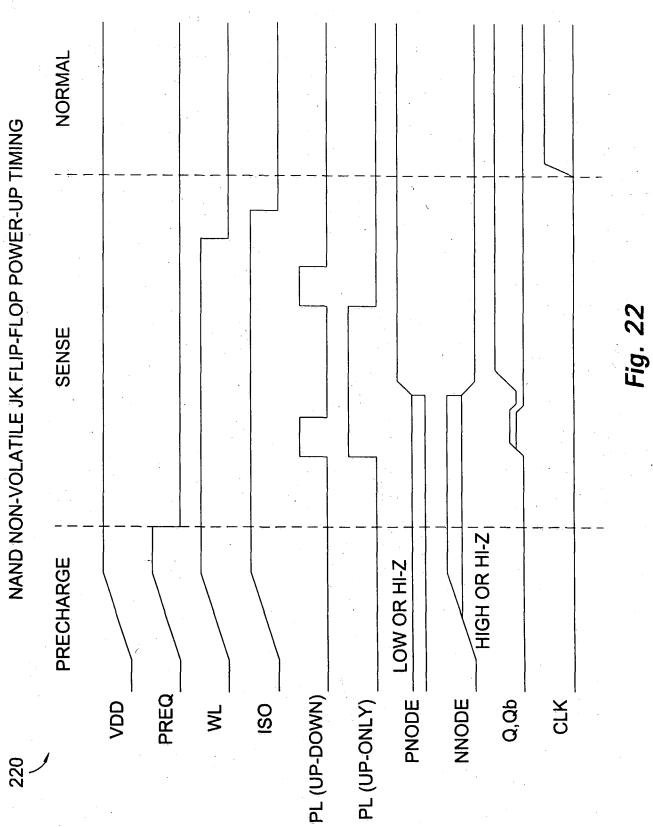


Fig. 21



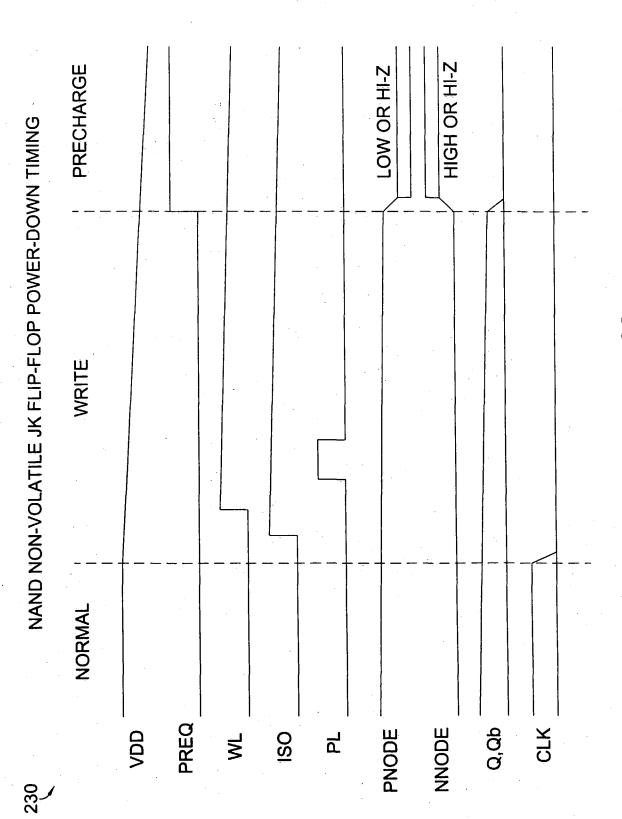
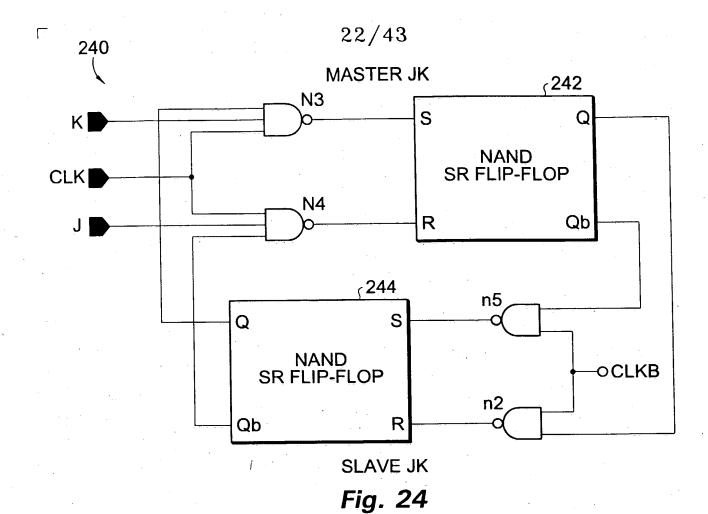
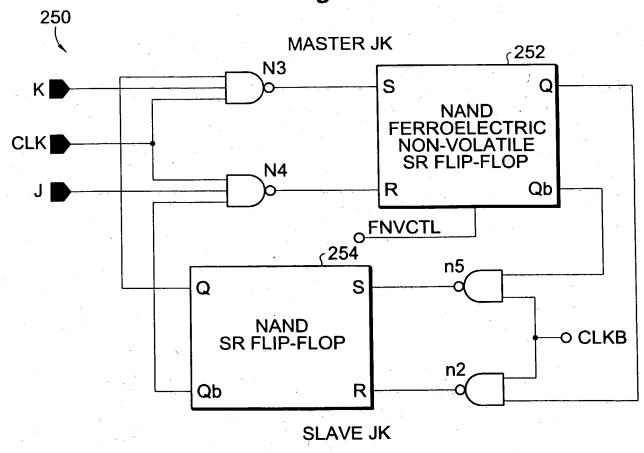


Fig. 23





Fia. 25

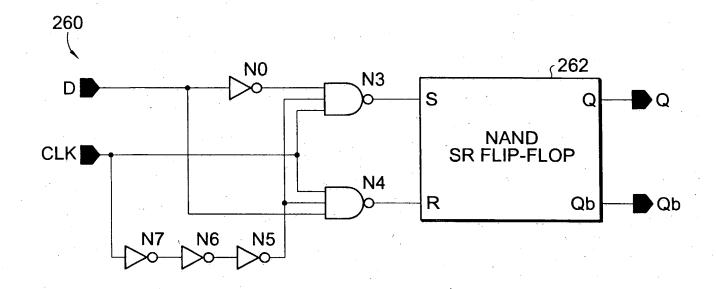


Fig. 26

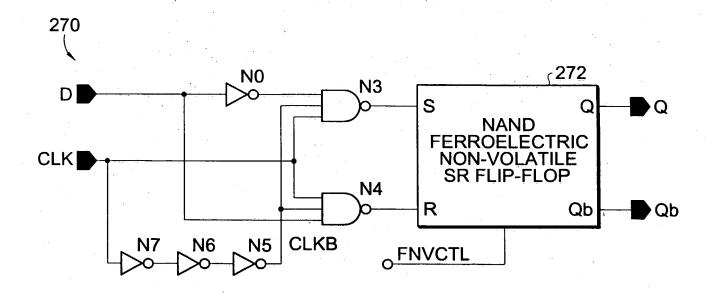


Fig. 27

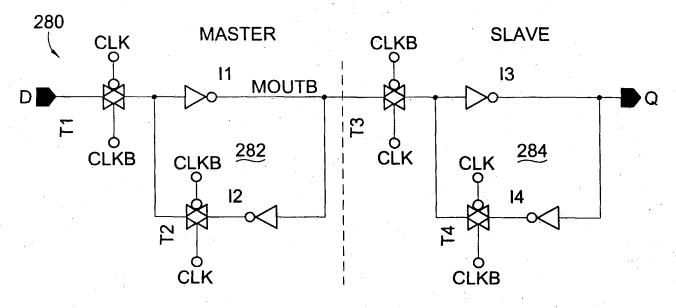


Fig. 28

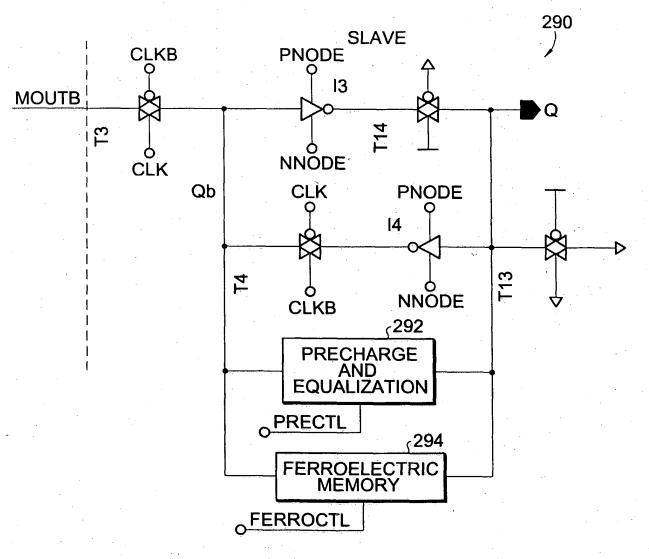


Fig. 29A

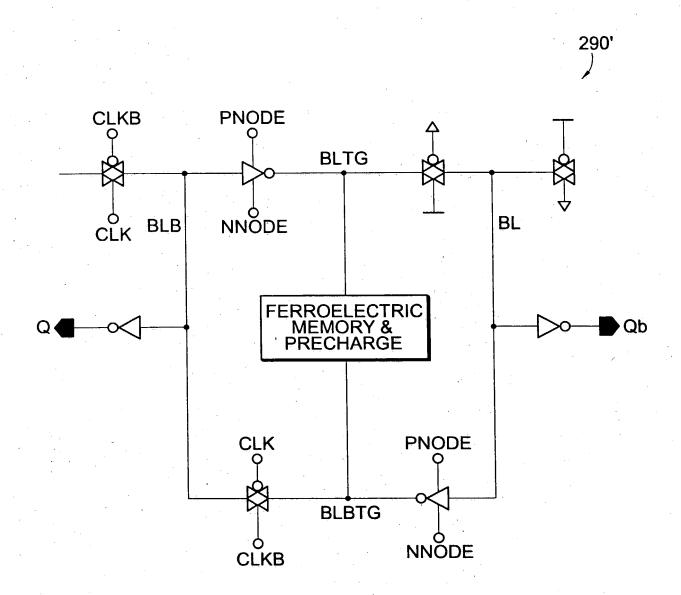


Fig. 29B

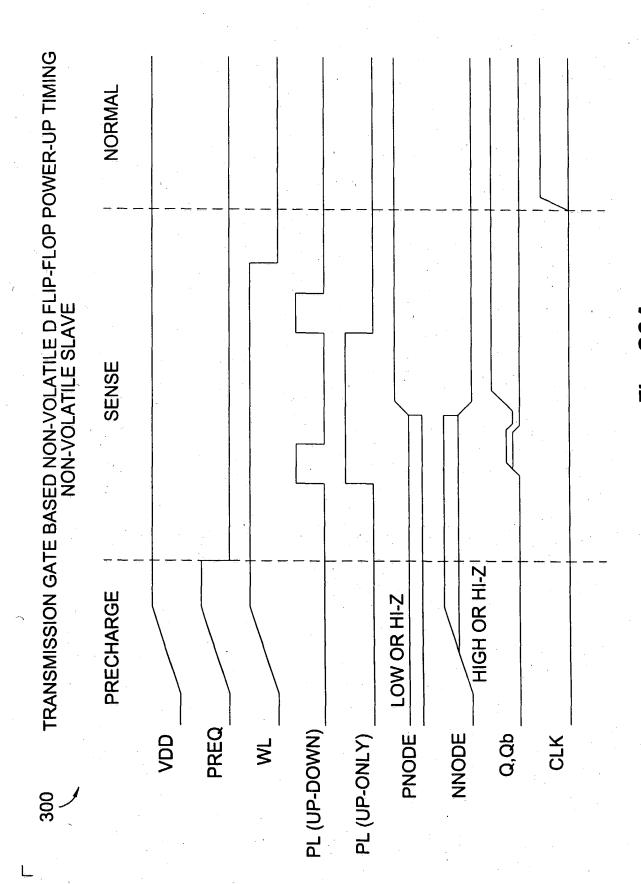
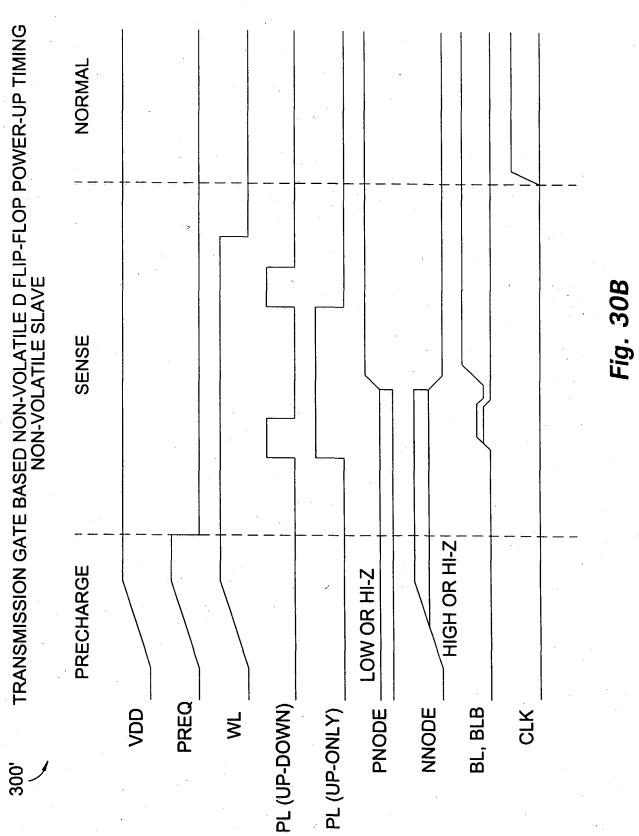


Fig. 30A

TRANSMISSION GATE BASED NON-VOLATILE D FLIP-FLOP POWER-DOWN TIMING **PRECHARGE** HIGH OR HI-Z LOW OR HI-Z WRITE NORMAL PREQ PNODE a,ab VDD CLK M۲ Ъ NNODE

Fig. 31A



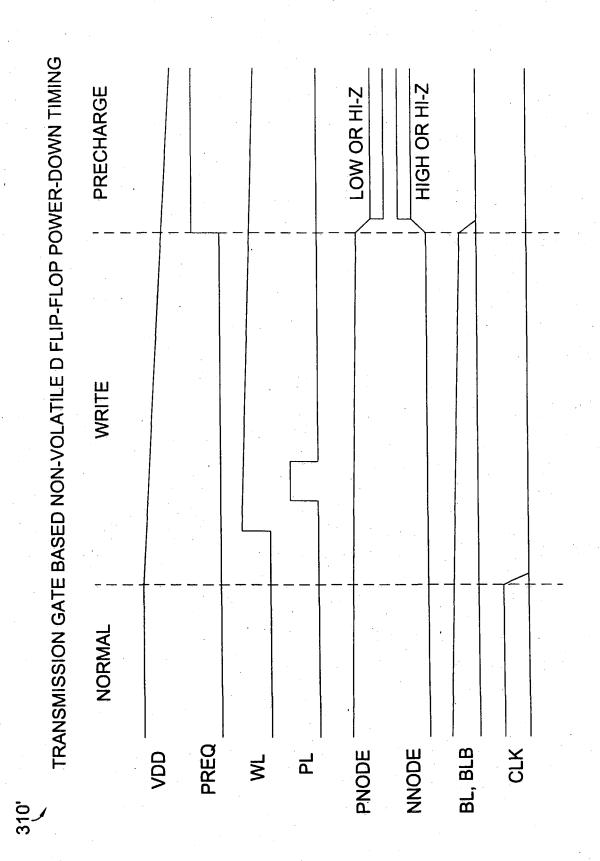
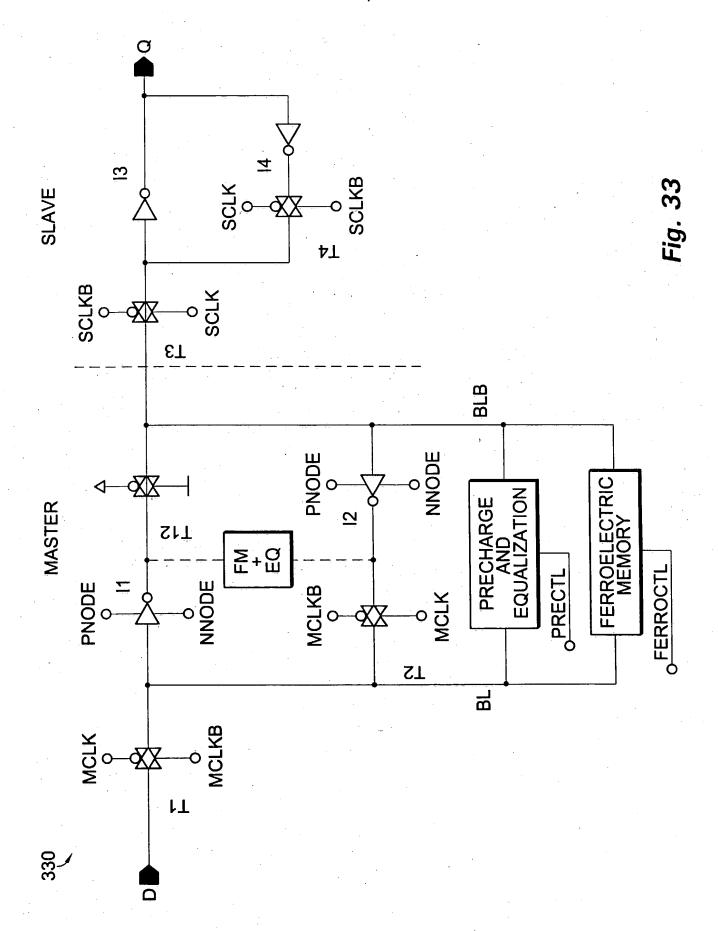


Fig. 31B



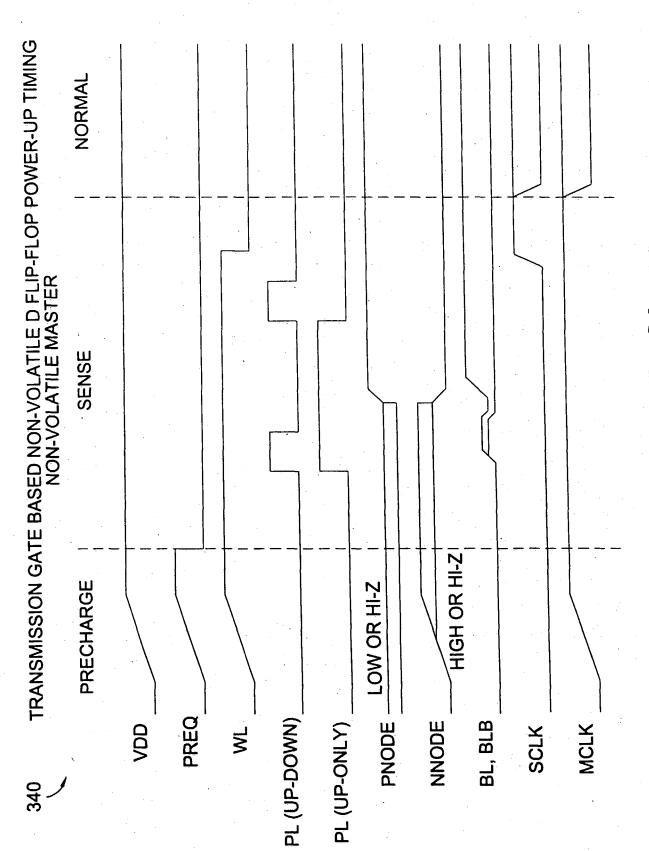


Fig. 34

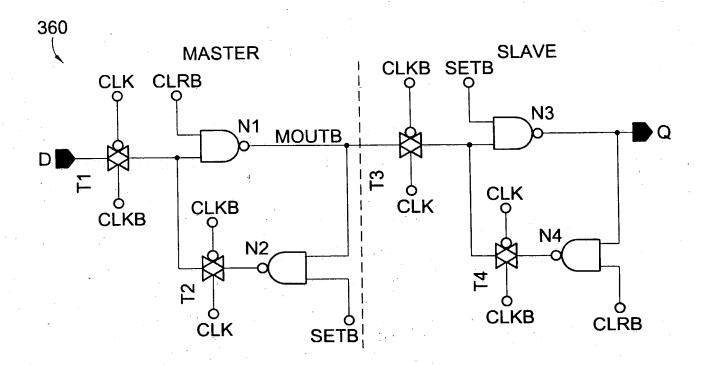


Fig. 36

•			
CLK	SETB	CLRB	Q
X	0	0	1
X	0	1	1
X	1	0	0
X	1 )	1	QLAST
1	1	1	D

Fig. 37

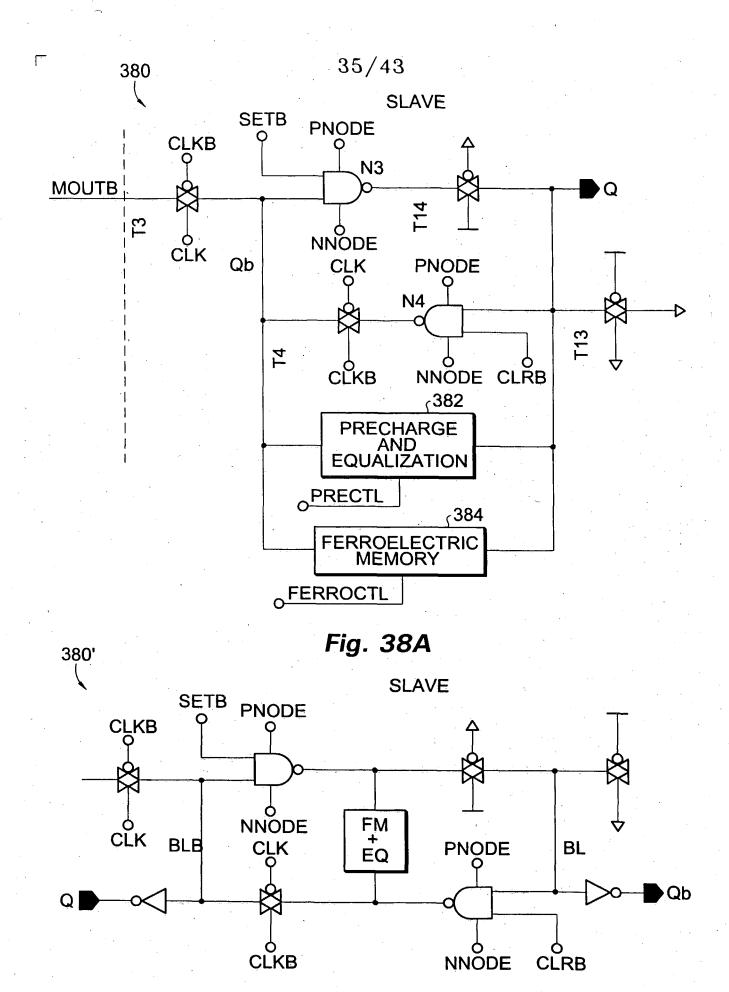
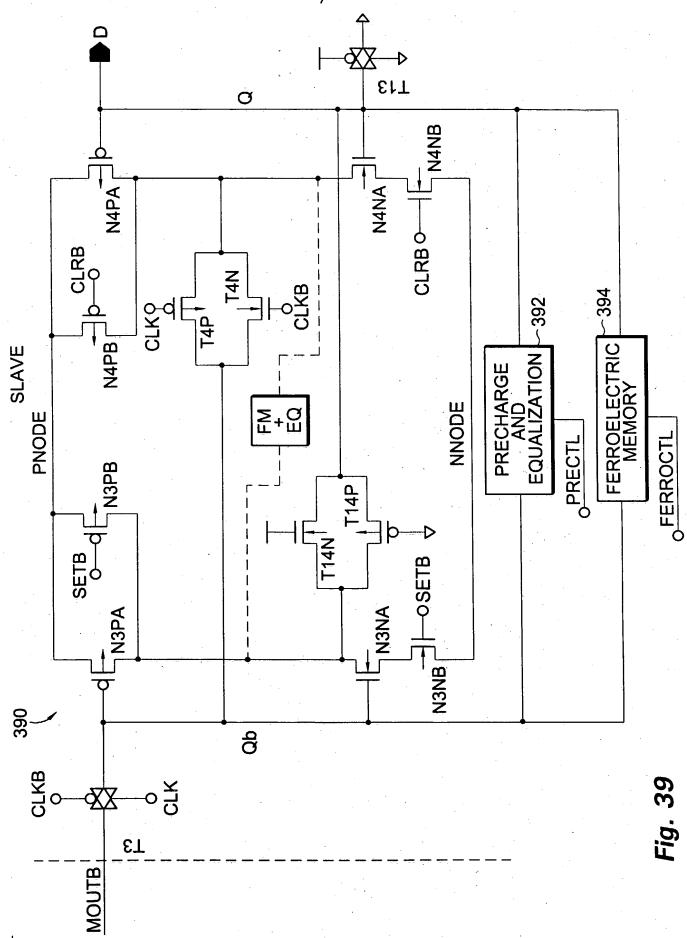


Fig. 38B



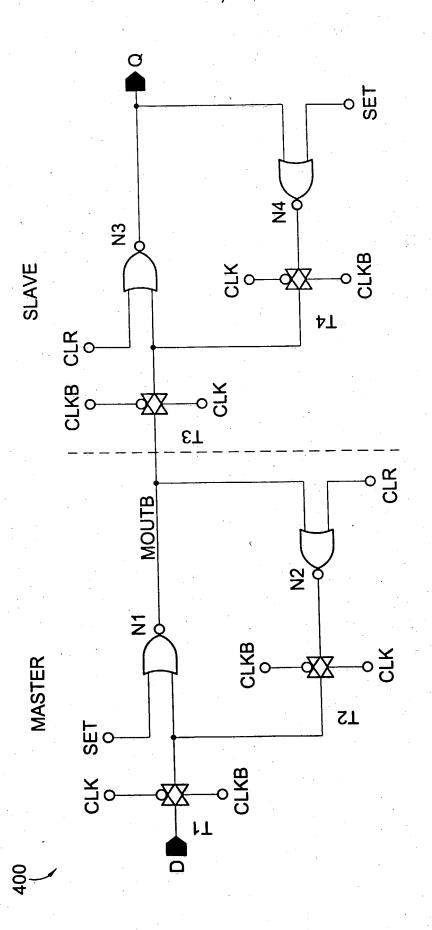
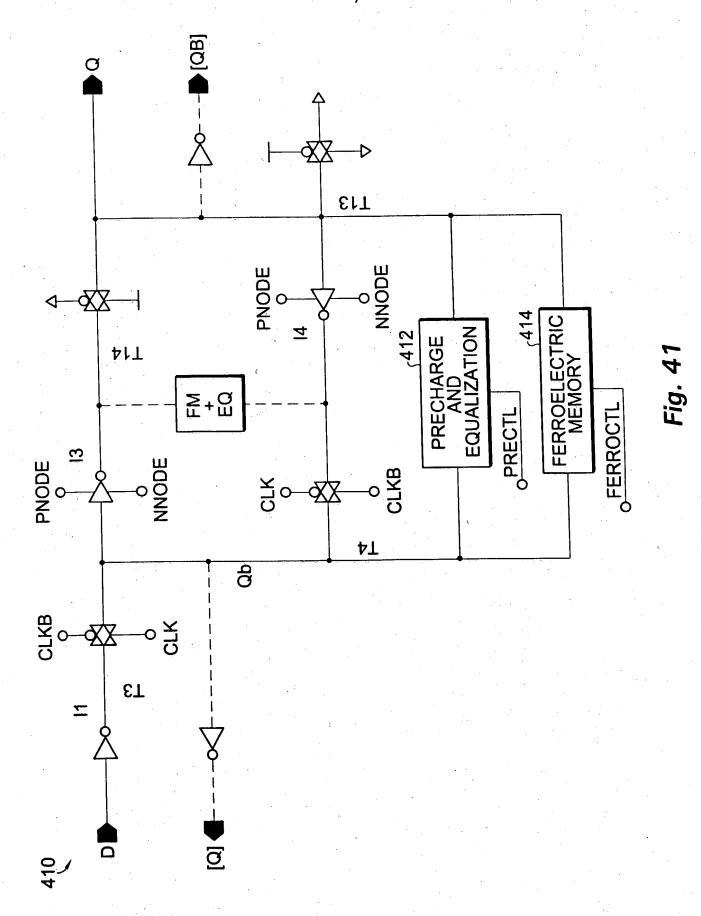


Fig. 40



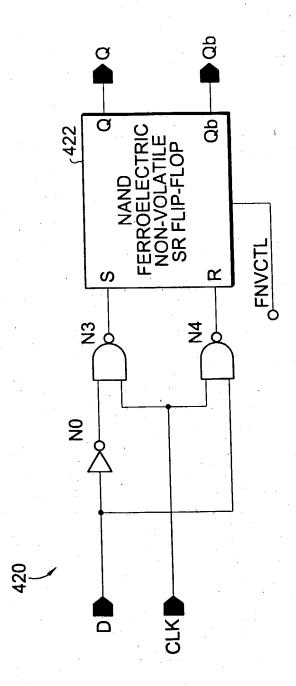
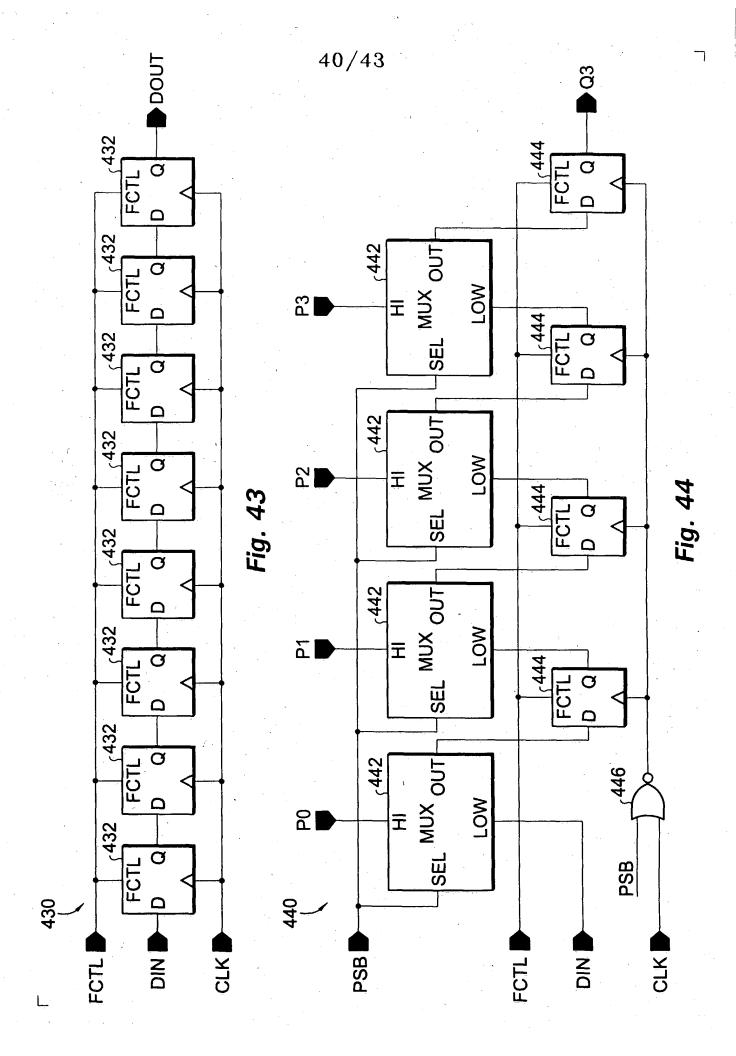
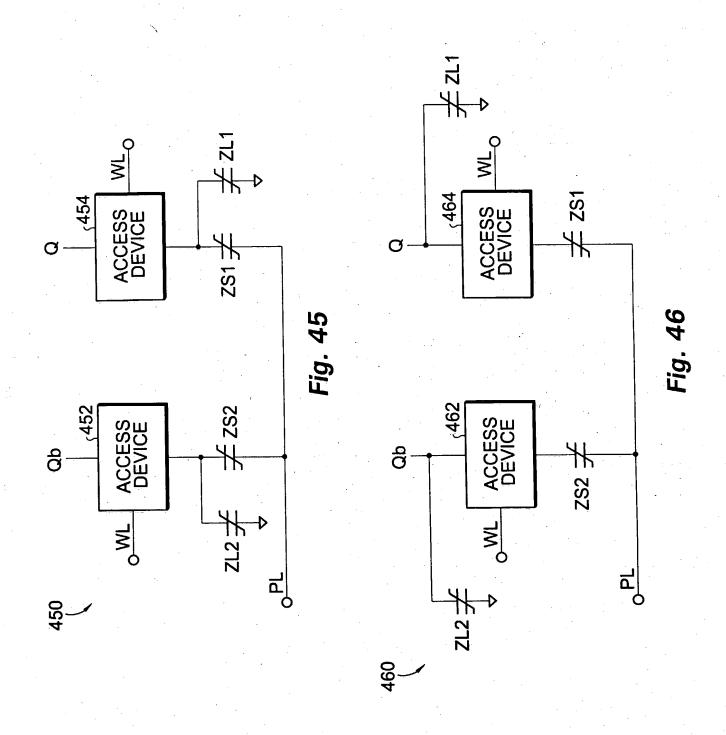
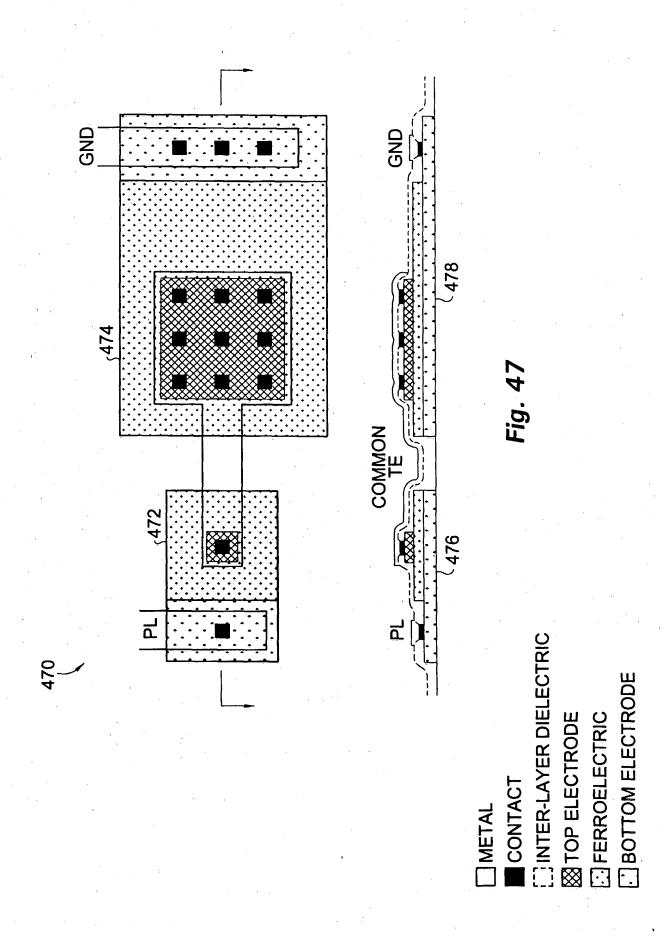


Fig. 42







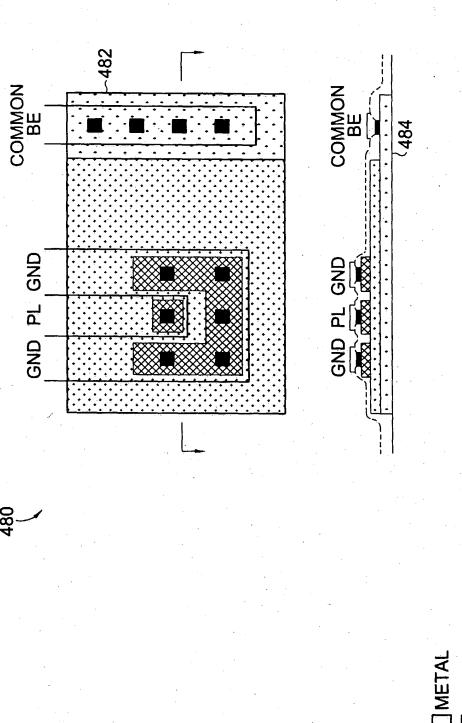


Fig. 48

] INTER-LAYER DIELECTRIC CONTACT

FERROELECTRIC **™TOP ELECTRODE** 

BOTTOM ELECTRODE